Summary of Changes to the ESDA/JEDEC Human Body Model Standard for 2011

Drafted by Members of the JEDEC/ESDA Joint Working Group for HBM, December 2010

The first Joint ESDA/JEDEC HBM standard was issued in 2010 with the primary goal to merge two separate methods. This was the first step in a two-step process. It was entirely focused on harmonizing differences between the existing ESDA and JEDEC methods and did not address new methodologies or next generation issues. These issues are addressed in the new 2011 revision of joint standard JS-001. The purpose of this summary is to describe briefly the most important changes in this revision and the motivation for implementing them.

This revision was made in response to well-documented critical issues which are intrinsic to the relay-matrix HBM testers. When these machines were first introduced over twenty years ago, these issues were not a large problem because devices had relatively low pin count and were considerably less complex. The new standard is needed because device scaling and complexity have brought the industry to the point where the shortcomings of the original test method are having serious effects on test accuracy, productivity and cost, and ever increasing testing times. Thousands of ESD pulses are now applied to a single IC component. This would not be seen in any real world ESD environment and it has been shown to induce a premature wear out failure mechanism (such as threshold shifts due to accumulative charge trapping in gate oxides). Test times have significantly increased due to the continued growth in pin count (see Figure 1) and the number of independent power supplies (see Figure 2), as IC components increase in their functionality due to the growth in system-on-a-chip (SOC) and multi-chip packages (MCP). The uncontrolled (parasitic) interaction between ICs and testers have increased due to the continued technology scaling, the decrease in power supply voltages, and the complexity of high pin count HBM test equipment. The IC-tester interactions can produce false device failures causing improper ESD sensitivity classifications. Significant changes to the existing HBM test method are therefore clearly needed to address the HBM testing challenges of modern ICs.

The changes in the 2011 version will be very effective in addressing the most critical problems. However, many users may choose not to change their methods if their devices are not on the leading edge of scale and complexity. Also, the new methods will require some changes to procedures that have become automated and familiar. Adjustments will be needed in device information provided by designers to the personnel executing the tests and new means for generating stress test programs will evolve. Given these transition issues, the 2011 version allows either the new or the legacy method to be used. As the industry becomes accustomed to the new methods, it is anticipated that they will gain wider adoption. It should also be noted that

there have been no significant changes to the actual stressing method. The current waveform definition and the procedures for verifying compliance remain the same.

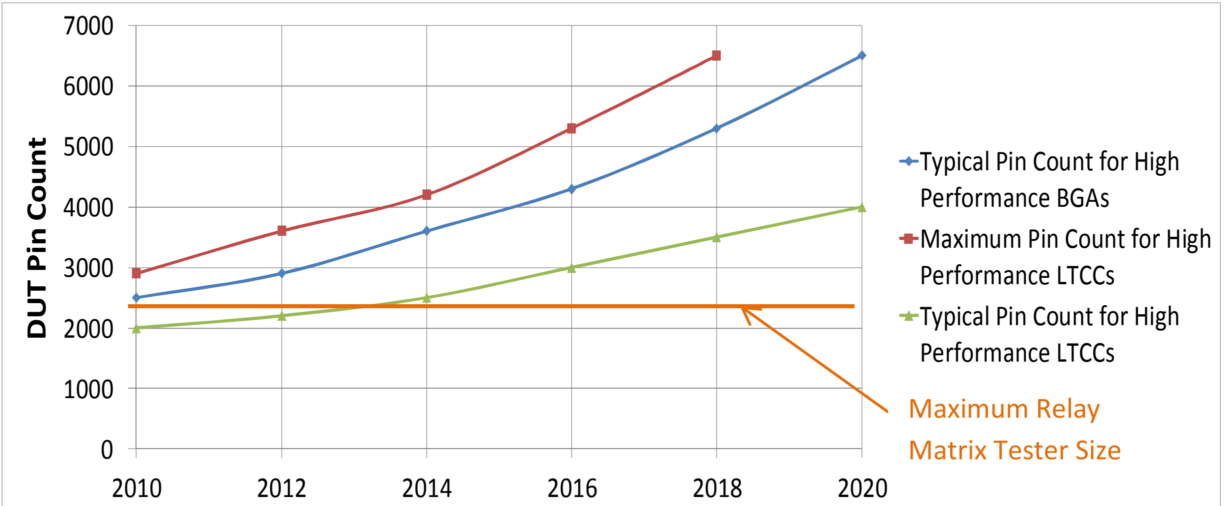

Figure 1: Pin count data extracted from The International Technology Roadmap for Semiconductors, 2010 Update

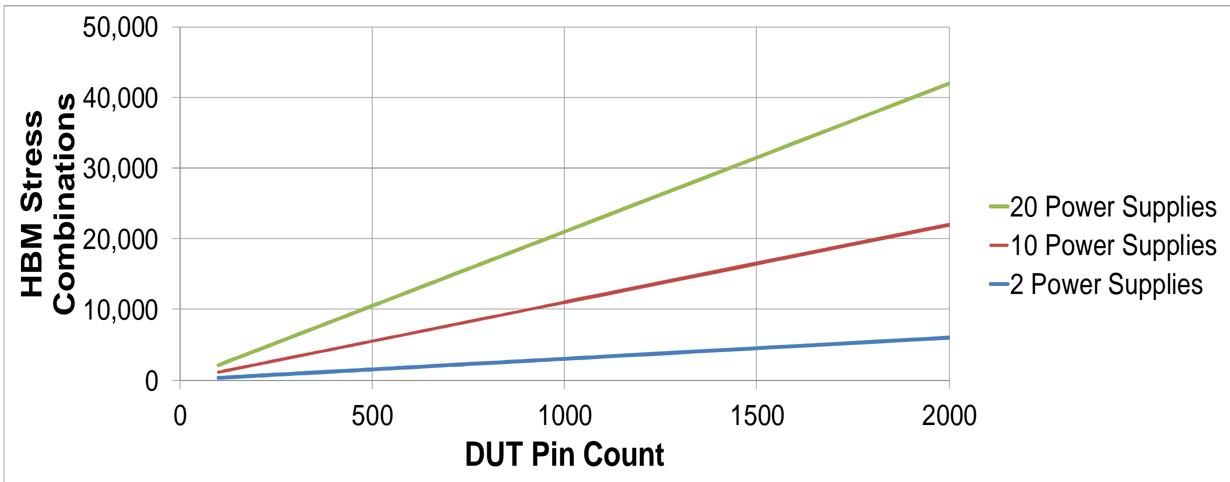

Figure 2: Stress combinations increase with both the DUT pin count and the number of DUT power supplies

To provide a better HBM test method the updated standard has made changes in the following areas:

1. Reduce the HBM test time and premature HBM wear out failure mechanisms by changing the total number of stress pin combinations by:
   a. Simplifying the I/O-to-I/O pin combination to a reduced set of pin combinations.
   b. Removing stressing of I/O pins to power supplies that are outside their functional local power domain.
2. Add options to decrease the parasitic interaction of the IC package device under test (DUT with the HBM tester by:.
   a. Enabling the two-pin automated tester option.
   b. Applying pulses of a single polarity for supply pin-to-supply pin testing.

The four major changes made in the JS-001-2011 revision are:

1) Most non-supply to non-supply (I/O-to-I/O) eliminated - testing is limited to differential pairs

The existing HBM pin combination I/O-to-I/O (2010 Version, Table 2, row N+1) applies HBM stresses to each I/O pin on terminal A and groups together all of the other I/O pins to terminal B and grounds those pins.

This pin combination has the following drawbacks:

1. Represents a small fraction (<1%) of all possible I/O-to-I/O pin combinations for package with > 100 pins.
2. Was introduced as a compromise due to the excessive test time required to stress all possible I/O-to-I/O pin combinations.
3. Does not represent any possible real ESD situation as the simultaneous grounding of all I/Os in the test or assembly areas is unrealistic.
4. Is redundant to the I/O to supply pin group combinations in most cases.
5. Few failures are found with I/O-to-I/O testing that aren't identified with I/O to power rail testing (and these are mostly identified with differential pairs)
6. May not detect weak ESD paths between I/O pin pairs because the one-to-many I/O test has so many additional paths possibly allowing current to avoid the weak pairs.
7. May lead to false failures in a few cases [1].

This change has a precedent. The I/O-to-I/O stress requirements were removed from the JEITA HBM standard, EIAJ ED-4701/300-2, in 2001 and there have been no problems associated with this change. However, there are known and understood I/O-to-I/O failures possible in some device designs, therefore the JS-001-2011 standard retains the I/O-to-I/O testing for those cases, which include differential pairs. A test targeted towards these pin pairs is expected to provide better information and will likely reduce test time for the IC device.

2) Eliminating "Cross-Domain" testing of non-supply (I/O) pins

Many devices have multiple supplies organized in sets or domains that power different sections of the IC. The typical ESD current paths from an I/O (non-supply) pin to power groups outside its local power domains is from the I/O pin to power rail(s) of its local domain through its power–ground clamp and then between the ground diodes to the different supply domains. As the HBM stress currents repeatedly flow through this current path cumulative stresses can occur on any cross domain CMOS logic gate that interfaces between the different power domains. This cumulative stress can create unrealistic premature wear out mechanisms due to trapped charge or Vt shifts [2].

In JS-001-2011, this unwanted cumulative stress is greatly reduced. This "cross-domain" stressing is eliminated by requiring that signal pins are stressed only to their associated local supply pin groups. Then, all of the supply pins of each group are stressed to all of the other supply pin groups (as is also done in the current method). Thus the current paths from any I/O pin to any power pin are tested in two steps. This change significantly reduces the total number of pin combinations required to test a device, thereby saving significant HBM test time and it also eliminates cross domain wear out failure mechanism. To take advantage of this new set of pin combinations, additional information is needed to make the association of signal pins to their local supply groups.

3) Pin combinations for Two-Pin Testing

The simplest and most realistic HBM test is to stress all two-pin combinations. Relay-based HBM testers have been engineered to test pins in the one-to-many combinations using relay switching to reduce the total number of combinations required. However, the unintended parasitics of this tester configuration have been shown to affect test results, especially with shrinking device geometries [3]. Issues regarding false failures from these testers for certain device types have been published [4].

The proposed revision (JS-001-2011) simply permits the existing one-to-many pin combination sets to be divided into one-to-one sets so that all devices can be stressed in two-pin combinations. This is an especially important option as it is suspected that tester parasitics produce false failures [Section 6.6 of JS-001-2010].

4) Using "Single Polarity" supply-to-supply stressing

This change addresses problems that occur due to the parasitic relay matrix capacitance of unselected pins. It also removes some redundant pin combinations. We address the redundancy first. When HBM stress is performed between device supplies, each supply pin is tested to all other supply pin groups. This means that each pin of supply A is tested to supply pin group B and also each pin of supply B is tested to supply pin group A. The redundancy of testing both A to B and B to A with both polarities can be eliminated by testing pins in both directions with a single polarity. Stressing with positive pulses from A to B and from B to A uses ESD current paths similar to stressing from A to B with both positive and negative pulses and

also B to A with both polarities. The option for using a single (either positive or negative) polarity allows the stress program to minimize the impact of the interaction between the device and the tester parasitics [3,4]. The polarity can be selected to avoid forward biasing the diode clamps that connect voltage rails to I/O pins, and thereby can reduce the amount of the stress current that flows into tester parasitic capacitances. For most technologies the selection of positive polarity stress has proven to be the correct choice. Reducing the DUT-tester interactions allows most of the current that flows from the tester's Terminal A to be returned through Terminal B, more closely simulating a real event and properly activating the ESD protection circuitry.

Conclusion

We recognized that any change to a test standard, even when that change increases accuracy, may produce differences in the HBM test results for some IC devices. The changes introduced in this new revision are optional but preferred; IC devices that were previously classified by the JS-001-2010 may continue to use that classification. Many, but not all, devices will have the same classification when tested according to JS-001-2010 or JS-001-2011. For the devices that will have different classifications, the classification using the improved pin combinations of JS-001-2011 should be used..

Bibliography

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